

Appl. No.: 09/838,078
Amdt. dated June 22, 2004
Reply to Office action of April 16, 2004

REMARKS/ARGUMENTS

In the Office Action dated April 16, 2004, the Examiner: (1) requested a list of copending applications to be updated with current status information; (2) objected to the order of one of the claims; (3) objected to claims 8 and 17 for various informalities; (4) rejected claims 1, 8 and 11 under 35 U.S.C. § 112, second paragraph; (5) rejected claims 1-13 and 15-20 as anticipated by Rotenberg; and (6) rejected claims 14 and 21 as obvious over the combination of Rotenberg and Patterson. In this Response, Applicants amend the specification to update the list of copending applications and amend claims 1, 8, 9, 11, and 17. Based on the arguments and amendments contained herein, Applicants submit that all claims are in condition for allowance and respectfully request reconsideration.

I. CLAIM OBJECTIONS

The Examiner objected to claim 8 as being separated by claims 4-7 from claim 3 (on which claim 8 directly depends). Applicants are unclear as to how this issue should be resolved. The Examiner did not require correction and Applicants assume that the claims can and will be renumbered when the case is allowed if the Examiner so chooses.

The Examiner also noted a typographical error with the word "temporary" in two instances in claim 8. This word has been changed to "temporarily." Further, the Examiner requested clarification of the first instance of the acronym "SRT" in claim 17. Specifically, the Examiner requested that SRT be spelled out in its full form—i.e., "simultaneous and redundantly threaded." Applicants complied with the Examiner's request.

II. THE § 112, SECOND PARAGRAPH, REJECTIONS OF CLAIMS 1, 8, AND 11

The Examiner rejected claim 1 under § 112, second paragraph, because, according to the Examiner, "[it] is unclear how the processor can correctly use the outcomes for one branch instruction to predict the outcome in a second, seemingly unrelated branch instruction in a different program thread." Applicants amend claim 1 to refer to "corresponding" branch instructions.

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The Examiner also noted several antecedent basis issues with regard to various terms in claims 8 and 11. These issues have been addressed by amendment.

III. THE ART REJECTIONS

The Examiner used Rotenberg in rejecting all pending claims. In section 1.2 Rotenberg discloses an "active" instruction stream (A-stream) and a "redundant" instruction stream (R-stream). The results of the A-stream are pushed onto a "delay buffer" (Figure 2). "As the R-stream is fetched and executed, its committed results are compared to those in the delay buffer. A fault is detected if the comparison fails... . Rotenberg, first two paragraphs of section 1.2. Thus, the delay buffer in Rotenberg is used to check the results of the instructions in the A-stream and R-stream to detect the occurrence of errors. Rotenberg also discloses that the delay buffer is implemented as a First-In-First-Out ("FIFO") buffer and that the delay buffer is used to cause the R-stream to lag behind the A-stream. See end portion of section 1.4.

Applicants amend claim 1 in several regards. First, the "I/O controller" and "I/O device" limitations have been removed as being unnecessary for patentability. These amendments naturally were not made to overcome any art of record nor does they narrow the scope of the claim. By removing the I/O controller and I/O device references, the claim is broadened in those respects.

Applicants also amend claim 1 to overcome Rotenberg. Applicants amend claim 1 to specify that the SRT processor comprises a "counter" and that "said counter causes instructions in a trailing thread to be fetched after corresponding instructions in a leading thread." Rotenberg does not teach or even suggest the use of counter in this regard. At most, Rotenberg teaches a FIFO buffer (i.e., the delay buffer in Figure 2) to cause the R-stream to lag behind the A-stream. At least for this reason, claim 1 and its dependent claims are patentable over Rotenberg.

Applicants amend claim 9 to require the SRT processor to include a counter that "causes instructions in the second program thread to be fetched after corresponding instructions in the first program thread are fetched." As explained

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above, Rotenberg does not teach or even suggest such a counter. At least for this reason, claim 1 and its dependent claims are patentable over Rotenberg.


Applicants amend method claim 17 to also require "decrementing a counter when the leading thread commits an instruction and incrementing the counter when the trailing thread commits an instruction." Rotenberg has no such teaching. At least for this reason, claim 17 and its dependent claims are patentable over Rotenberg.

The Examiner combined Patterson with Rotenberg to reject dependent claims 14 and 21. Claims 14 and 21 are patentable at least for the same reason as their independent claims. Patterson does not satisfy the deficiencies of Rotenberg identified above with regard to the independent claims.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Respectfully submitted,


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